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(71) Applicant: **CSELT Centro Studi e Laboratori Telecomunicazioni S.p.A.**
Via Guglielmo Reiss Romoli, 274
I-10148 Turin (IT)

(72) Inventor: **Bella, Valter**
Corso Peschiera, 255
Torino (IT)
Inventor: **Finotello, Andrea**
Via Gobetti, 3
Settimo Torinese (TO) (IT)
Inventor: **Galgani, Danilo**
Piazza Mattirolo, 8
Torino (IT)
Inventor: **Gandini, Marco**
C.so Svizzera, 60
Torino (IT)

(74) Representative: **Riederer Freiherr von Paar zu Schönau, Anton et al**
Lederer, Keller & Riederer,
Postfach 26 64
D-84010 Landshut (DE)

(54) CMOS technology high speed digital signal transceiver.

(57) CMOS technology high speed digital signal transceiver, in which the receiver has a clock signal extraction circuit, which is capable of self-aligning on incoming data with no spurious locks. Utilizing the PLL technique, the circuit generates a clock signal locked to the incoming signal utilizing a local oscillator, voltage-controlled by two feedback loops, a main one for frequency and phase corrections and a secondary one for phase correction. Moreover, original circuit solutions for the phase detectors and the low-pass filters are also envisaged.

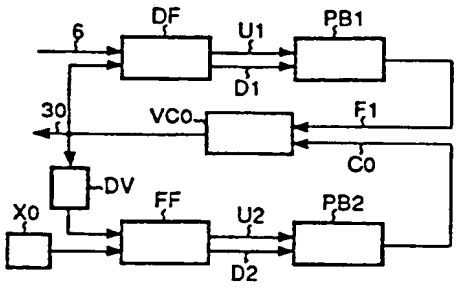

Fig. 4

EP 0 658 995 A1

The present invention concerns the devices for electronic systems in which digital signals have to be exchanged between equipment located in places that are separated by some distance and in particular it refers to a high-speed, CMOS technology, digital signal transceiver, which can be realized as an integrated circuit on a single chip.

It is well known that when digital signals in parallel form have to be transmitted at a certain distance, it is preferred to convert them in serial form so as to be able to utilize a single transmission line, instead of as many lines as are the bits of the parallel signal, for instance eight. The signal to be transmitted must furthermore be appropriately coded in order to minimize its sensitivity to any interference which may hake been collected by the transmission line and to enable the receiving apparatus to check the correctness of the received datum. Naturally, upon reception the signal has to be reconverted into the original form in order to be utilized.

Digital signals to be transmitted, coded in a parallel mode and, generally, in NRZ (Non Return to Zero) format, must undergo a first coding of the 4B/5B type, which, by making a 5 bit block correspond with each 4 bit block, allows to enlarge the number of transitions of the transmitted signal. In particular, this coding guarantees the occurrence of at least one logic level transition for each 4 bits transmitted, avoiding the risk of a loss of synchronism of the receiving equipment in the presence of long stays at the same logic state. Moreover, the possible reception of one of the 16 not utilized 5-bit codes may be used for the detection of errors in the received signal.

After the 4B/5B coding, the parallel signal has to be converted into series mode and into the NRZI (Non Return to Zero Inverted) format, adopted internationally.

The NRZ/NRZI format converter causes the digital signal to be changed over between the two logic states, at the clock signal rate, when the NRZ signal remains at level one, whereas it causes it to stay at 0 or at 1 (depending on the last transition performed), when the NRZ signal is at logic state 0.

In reception, it is necessary to read correctly the received data, extracting from them the clock signal for the detection, and thus perform the inverse conversion and decoding operation, checking for the presence of any possible transmission errors.

The extraction of the clock signal is usually performed utilizing a PLL (Phase Locked Loop) circuit, which uses as a reference signal the same numerical signal arriving to the receiver and provides at the output side a clock signal at a frequency that is twice the bit rate. The arriving signal constitutes a good reference signal if it is rich in level transitions, so that its frequency spectrum has a precise component at the bit repetition frequency. This component is usually extracted by means of pass-band filters of the LC or SAW (Surface Acoustic Wave) type. These filters are rather bulky, they cannot be integrated with circuits on the same chip and they reduce the flexibility of the device, as they do not allow frequency excursion.

Another difficulty derives from electromagnetic compatibility problems due to the need to integrate on the same chip at least two PLL circuits, one in reception for the extraction of the clock signal and another one in transmission for the multiplication of the system clock signal for the serialization of the digital signal. Naturally on the same chip there may be more than one transceiver, and several PLL circuits, each with its own VCO (Voltage Controlled Oscillator), operating at radio frequency simultaneously with the others and thus being a source of electromagnetic radiation. Therefore it is necessary to adopt a precise topological strategy, at the design stage, concerning the placement of the circuits on the chip, in order to minimize disturbances and interferences.

Finally, the device has to be able to operate at rather high bit rates, which currently are around 200 Mbit/s, maintaining at the same time reduced power consumption.

A transceiver that is able to carry out the aforementioned functions, called HOT-ROD, has been realized by Gazelle in GaAs technology, which allows to reach considerable bit rates, but is very expensive and inefficient: the ratio between the devices that are actually in operation and those produced is only about 20%, while for devices realized on silicon it reaches 80%.

A transceiver of this type may also be realized utilizing bipolar technology integrated circuits, such as those denominated SP9970 and SP9930 by GEC Plessey. The former integrated circuit contains a series-to-parallel converter, a parallel-to-series converter and a PLL that performs the multiplication by 10 of system frequency, whereas the latter one contains a PLL for the extraction of the clock signal and a NRZ/NRZI converter. Moreover, other circuits for the 4B/5B coding/decoding and the detection of errors are required.

With these circuits too the attainable bit rate is good, but the power consumption, typical of bipolar technology, is rather high.

Both examined solutions allow the extraction of the clock signal without the use of external filters, substituted by appropriate PLL circuits comprising a main loop (master) and a slaved one (slave), as described for example in the paper "A BiCMOS Receive/Transmit PLL Pair for Serial Data Communication", by Barry L. Thompson et al.. presented

at IEEE 1992 Custom Integrated Circuits Conference, or in the paper "A Self Correcting Clock Recovery Circuit", by Charles R. Hogge, published in the Journal of Lightwave Technology, no. 6, December 1985. The master loop recovers the fundamental frequency of the system starting from a reference frequency, while the slave loop brings about small phase corrections as a function of the received signal.

However, this type of PLL circuit presents some problems, as the two VCOs disturb each other, causing spurious locks.

These drawbacks are obviated by the CMOS technology, high-speed, digital signal transceiver, object of the present invention, which is realized on a single CMOS technology integrated circuit, has low power consumption and high working speed, all inputs and outputs have a low voltage swing, and the clock signal extraction circuit is able to self-align to data arriving with no spurious locks.

In particular, object of the present invention is a transceiver for high speed digital signals in CMOS technology, comprising a transmitter, in which the incoming parallel flow is coded in a code having a higher number of transitions, converted into serial form and coded in the line code, and a receiver, in which the incoming serial flow is decoded from the line code, converted into parallel form and decoded in order to re-obtain the original parallel flow, the generation of the clock signal for the aforesaid decoding operations from the line code and conversion into parallel form being performed by a block, characterized in that it comprises a local oscillator, voltage controlled by two feedback loops, the first of which comprises:

- a crystal oscillator;
- a binary divider, which divides the signal provided by the local oscillator;
- a phase-frequency detector, which operates on the signals provided by the binary divider and by the crystal oscillator, providing the outputs with signals at a suitable logic state, if the frequencies of the incoming signals are different, correction pulses at the appropriate instants, if the incoming signals have equal frequencies but are out of phase with respect to each other;
- a first low-pass filter, which receives the signals provided by a phase-frequency detector and controls the local oscillator; and the second feedback loop comprises:
- a phase detector, which operates on the signals provided by the local oscillator and on the incoming serial flow, providing at the output a third pulse reference signal and a fourth pulse signal, active for a time varying as a function of the phase error between the signals at its inputs;
- a second low-pass filter, which receives the signals provided by the phase detector and controls the local oscillator.

These and other characteristics of the present invention will be better clarified by the following description of a preferred embodiment thereof, given as a non- limiting example, and by the enclosed drawings wherein:

- Figure 1 is a block diagram of the digital signal transceiver;
- Figure 2 is a block diagram of the transmitter denoted by TX4 in Figure 1;
- Figure 3 is a block diagram of the receiver denoted by RX4 in Figure 1;
- Figure 4 is a block diagram of the clock signal generation block denoted by PR1 in Figure 3;
- Figure 5 is an electrical diagram of the phase detector denoted by DF in Figure 4;
- Figure 6 is a time diagram in which the main waveforms of phase detector DF of Figure 5 are represented;
- Figure 7 is a circuit diagram of a low-pass filter denoted by PB1 in Figure 4.

The digital signal transceiver, shown in Figure 1, comprises, on a single chip, 8-bit receiver RX8 and transmitter TX8, as well as 4-bit receiver RX4 and transmitter TX4, electrically separated. Both transmitters convert the parallel data applied to inputs 1 and 2 into serial data, which they provide to outputs 3 and 4. The receivers perform the inverse operation, receiving serial data at inputs 5 and 6 and providing parallel data to outputs 7 and 8.

The transceiver is thus suitable for performing point-to-point interconnections, transferring on a single wire information coming from parallel connections at 4 and/or 8 bit. In the transmission phase, two subsequent codings are performed, i.e. the type 4B/5B one and the one from NRZ to NRZI, in order to satisfy the specifications of international standard FDDI (ANSI), valid also for optical fiber transmission.

The transmitters have two control wires available: reset wires 9 and 11 and wires 10 and 12, which allow the generation of a synchronism word, useful in defining a transmission protocol compatible with the current ATM (Asynchronous Transfer Mode) system. The receivers have one reset wire 13 and 14 available.

Figure 2 shows the block diagram of 4-bit transmitter TX4. The block diagram of the 8-bit transmitter is entirely similar, so it shall not be described in detail, but rather the main differences shall be pointed out.

The 4-bit word incoming on connection 1 is carried to a register REG1, which transfers them in synchronism with the system clock signal present

on wire 20 to a coding circuit COD1, which performs the 4B/5B coding. The clock signal frequency is multiplied by 5 (it is instead multiplied by 10 in the 8-bit transmitter) by means of a PLL (Phase Locked Loop) circuit, indicated as PT1. Thus, on wire 21 a fast clock signal is obtained, which is brought with the slow clock signal to a parallel-to-series converter PISO1, which provides on output wire 22 a data flow of the NRZ type. The subsequent conversion from NRZ to NRZI is performed in block ZZI1, which provides as output on wire 3 a signal that may be sent over a suitable electrical transmissive means to the remote receiver. All blocks of the transmitter may be reset with a single command, sent by means of suitable wires, which are not shown.

In 4-bit receiver RX4, whose block diagram is illustrated in Figure 3, operations inverse to the ones performed in the transmitter are carried out. In addition, the receiver recovers the fast clock signal from the flow of incoming data. This is the most critical operation in a high-speed data receiving system, because of the presence of more than one harmonic in the incoming signal, and thus of the possibility that a harmonic may be erroneously considered as a reference frequency. The circuit for the generation of the clock signal, adopted in the present receiver, uses a PLL circuit of innovative characteristics, which allows to avoid the use of band-pass filters tuned to the reference frequency.

The serial flow arrives from the transmission line to input 6 of the receiver and undergoes decoding from NRZI to NRZ in the ZIZ1 block. Simultaneously, it is also sent to the generation block of the clock signal PR1, which makes available in output on wire 30 the fast clock signal. This signal is sent together with the NRZ flow provided by block ZIZ1 to a series-to-parallel converter SIPO1, which provides in output a parallel 5-bit flow. The subsequent 5B/4B decoding circuit DC01, controlled by the system clock signal present on wire 20, performs the second conversion from 5 bit to 4 bit. Thus, the parallel signal originally applied to the transmitter is re-obtained, and it is sent to an output register REG2, also controlled by the system clock signal on wire 20, and made available in output on connection 8.

The clock signal generation block PR1 is represented in Figure 4. It is based on the PLL (Phase Locked Loop) circuit, which, as it is well known, synchronizes in phase and frequency the signal generated by a local oscillator to a reference signal. This is achieved by operating the comparison between the reference signal and the local oscillator signal, suitably divided, and utilizing the error signal obtained, deprived of the alternate current component, to control the local oscillator in feedback.

The block PR1 uses a particular PLL circuit, composed of a single voltage-controlled local oscillator, denoted by VCO, and of two feedback loops.

The main loop generates an error voltage of wide dynamics which it sends through wire CO to the VCO, determining its more important phase and frequency corrections. The slave loop generates a second error voltage of lower dynamics, which is sent on wire F1 to a second input of the VCO, determining its accurate phase correction.

The reference signal for the main loop is generated by a crystal-controlled oscillator, denoted by XO, of a frequency equal to 1/10 of the frequency of the clock signal to recover. This signal is compared with the signal generated by the VCO, suitably divided by 10 by a binary divider DV, in a phase-frequency detector FF. The use of a phase-frequency detector is due to the fact that such detector does not allow lock conditions on frequencies that are harmonic to the desired one.

If the frequencies of the two signals are different, outputs U2 and D2 of detector FF, sensitive to the fronts of incoming signals and not to their duty cycle. stay blocked at an appropriate logic state. Low-pass filter PB2 placed in cascade emits, as a consequence, a continuous correction voltage that brings the frequency of the signal exiting DV to the same frequency of the reference signal exiting XO. In the iso-frequency condition thus reached, outputs U2 and D2 of FF behave as those of a normal phase detector providing correction pulses in the appropriate instants.

The low-pass filter PB2 has the task of providing at its output CO a dc voltage whose amplitude is the mean value of the pulses present at the outputs of the detector. It is a first-order low-pass filter, which has the peculiarity of containing within it, in integrated form, the resistance of RC network.

In such a way, a single connection toward the exterior is required to connect the capacitor. As this resistance must have a high stability, particular care must be devoted to dimensioning the transistors which embody it, making linear their resistive behaviour in the different operative points.

The slave loop comprises a phase detector DF, which compares the signal provided by VCO with the serial flow of data incoming on wire 6, providing the error pulses at its outputs U1 and D1. These pulses are sent to a low-pass filter PB1, realized in the same way as filter PB2, which makes available at its output F1 the fine correction voltage for the block VCO. The recovered clock signal is thus available in output from VCO on wire 30.

The electrical diagram of phase detector DF is shown in detail on Figure 5. It is an original circuit, which allows to generate a correction voltage ca-

pable of keeping the signal provided by VCO on wire 30 centered on the data signal arriving on wire 6.

The data signal is applied to input D1 of a D-type flip- flop, denoted by FFD1, which, receiving the clock signal at the input CLK, re-synchronizes it and makes it available at the output on wire 51. A second D-type flip- flop, denoted by FFD2, receives the data perfectly synchronized with the system clock signal, and, having as a reference the clock signal inverted by inverter INV, transfers it to the output on wire 52, delayed by half a cycle.

At output D1 of OR-exclusive circuit XOR2, which receives at its inputs the input and output signals of FFD2, there is for each transition of the incoming data a constant- duration pulse, equal to half the clock period.

Such pulse serves as a reference: if the datum coming into the detector were already perfectly aligned with the clock signal, then at output U1 of OR-exclusive circuit XOR1, which receives at its inputs the input and output signals of FFD1, there would be a signal having the same form as the one on D1, but leading by a half period.

If, instead, the incoming datum were not perfectly aligned, but, for instance, in phase lead, then the signal at output U1 would not vary, whilst the signal at the D1 output would remain active for a longer time. These signals would cause low-pass filter PB1 to supply at its output a voltage whose mean value varies proportionally to the phase difference, thus producing a decrease of the frequency of the clock signal generated by VCO (Figure 4).

Analogously, if the incoming data were lagging, then the signal at output U1 would remain identical, whilst the signal at output D1 would remain active for a shorter time producing an increase in clock signal frequency.

Figure 6 is a time diagram where the main waveforms of phase detector DF are represented. Each waveform is denoted by the number assigned to the wire where it is present. Waveforms 6a, 6b, 6c and U1a, U1b, U1c have to do with the signals present on wires 6 and U1 in the respective conditions of data aligned with the clock signal, leading data and lagging data.

Figure 7 represents the circuit diagram of one of the two low-pass filters utilized in the clock signal generation block, in particular filter PB1.

Pulse signals exiting the detector are applied to the two inputs D1 and U1, connected respectively to the gates of the two MOS transistors MNI and MPI, having the drains connected to each other and the sources connected to ground and to power supply source VDD.

These two N and P channel transistors operate as current sources for a couple of MOS transistors, N channel transistor MNRES and P channel transistor MPRES which realize resistance R of the RC network of the 1st order low-pass filter. The particular type of circuit allows to attain a compensation of the non-linearities of the MOS transistors and a behavior that is independent of the current direction.

Transistors MNRES and MPRES have their sources connected to each other and to the drains of the pair MNI, MPI and the gates connected to ground and to VDD. The drains are connected to wire F1 which goes to the control input of VCO (Figure 4) and to output terminal PAD of the integrated circuit, to which capacitor C, which determines the cutoff frequency of the filter, may be externally connected.

When on wire U1 there is a logic level 0, transistor MPI is driven into conduction, supplying current to transistors MNRES and MPRES, which charge the external capacitor C. A similar logic level applied to wire D1 would keep off transistor MNI, thus preventing its driving of the pair MNRES, MPRES.

On the contrary, the presence of a logic level 1 on wire D1 drives into conduction transistor MNI, so that the pair of transistors MNRES, MPRES may discharge to ground the external capacitor C.

On wire F1, connected to terminal PAD, there is thus a voltage that follows the mean value of the pulse signal provided by the detector, suitable for driving the controlled oscillator VCO (Figure 4).

It is evident that what has been described above was provided solely as a non-limiting example. Variations and modifications are possible without going out of the field of protection of the claims.

Claims

1. CMOS technology high speed digital signal transceiver, comprising a transmitter (TX4, TX8), in which the incoming parallel flow is coded (COD1) in a code having a higher number of transitions, converted into serial form (PISO1) and coded (ZZI1) in the line code, and a receiver (RX4, RX8), in which the incoming serial flow is decoded from the line code (ZIZ1), converted into parallel form (SIPO1) and decoded (DC01) in order to re-obtain the original parallel flow, the generation of the clock signal for the aforesaid decoding operations from the line code and conversion into parallel form being performed by a block (PR1), characterized in that this block (PR1) comprises a local oscillator (VCO), voltage controlled by two feedback loops, the first of which comprises:
   - a crystal oscillator (XO);

- a binary divider (DV), which divides the signal provided by the local oscillator (VCO);
- a phase-frequency detector (FF), which operates on the signals provided by the binary divider and by the crystal oscillator, providing the outputs (D2, U2) with signals at a suitable logic state, if the frequencies of the incoming signals are different, and with correction pulses at the appropriate instants, if the incoming signals have equal frequencies but are out of phase with respect to each other;
- a first low-pass filter (PB2), which receives the signals provided by the phase-frequency detector (FF) and controls the local oscillator (VCO); and the second feedback loop comprises:
- a phase detector (DF), which operates on the signals provided by the local oscillator (VCO) and on the incoming serial flow (6), providing at the output a third pulse reference signal (U1) and a fourth pulse signal (D1) which is active for a time varying as a function of the phase error between the signals at its inputs;
- a second low-pass filter (PB1), which receives the signals provided by the phase detector (DF) and controls the local oscillator (VCO).

2. Digital signal transceiver as in claim 1, characterized in that said phase detector (DF) comprises:
   - a first D-type flip-flop (FFD1), at whose data input (D) is applied the incoming serial flow (6) and at whose clock input (CLK) is applied the signal provided by the local oscillator (VCO);
   - a second D-type flip-flop (FFD2), at whose data input (D) is applied the output signal from the first flip-flop and at whose clock input (CLK) is applied the signal provided by the local oscillator (VCO) inverted by an inverter (INV);
   - two OR-exclusive gates (XOR1, XOR2), each with the inputs connected to the data input and to the output of one of the said flip-flops and with the outputs (U1, D1) connected to the outputs of the phase detector.

3. Digital signal transceiver as in claim 1 or 2, characterized in that said low-pass filters (PB1, PB2) comprise:
   - a first pair of complementary MOS transistors (MNI, MPI), whose gates are connected to the inputs (D1, U1), whose drains are connected to each other and whose sources are connected to ground and to the power supply (VDD);
   - a second pair of complementary MOS transistors (MPRES, MNRES), whose gates are connected to ground and to the power supply (VDD), whose sources are connected to each other and to the drains of the first pair and whose drains are connected to each other and to the output (FI), to which is also connected an external capacitor (C), which determines the cutoff frequency.

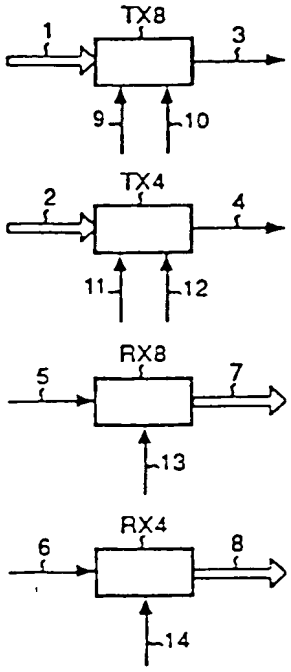

Fig. 1

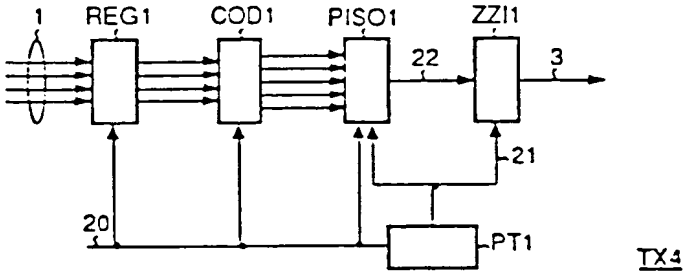

Fig. 2

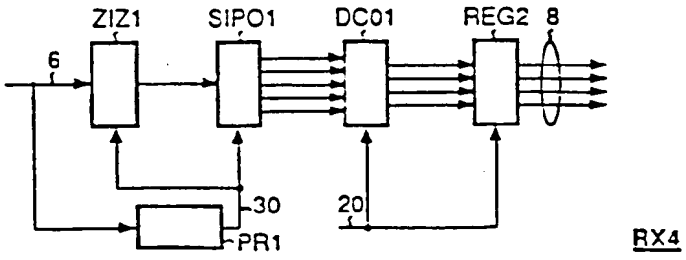

Fig. 3

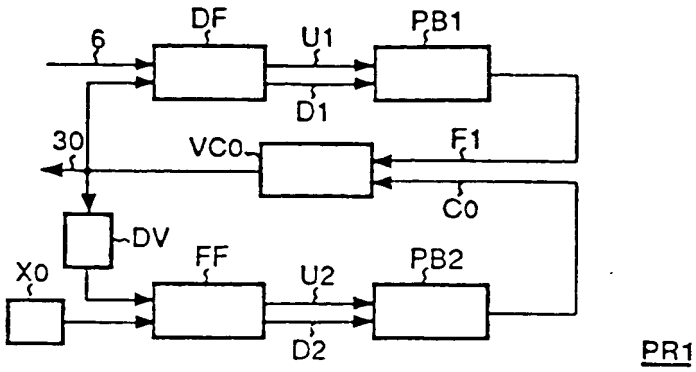

Fig. 4

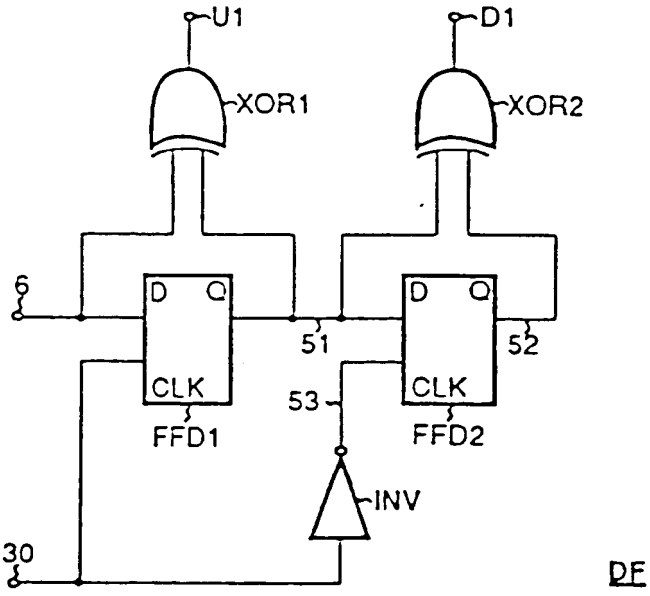

Fig. 5

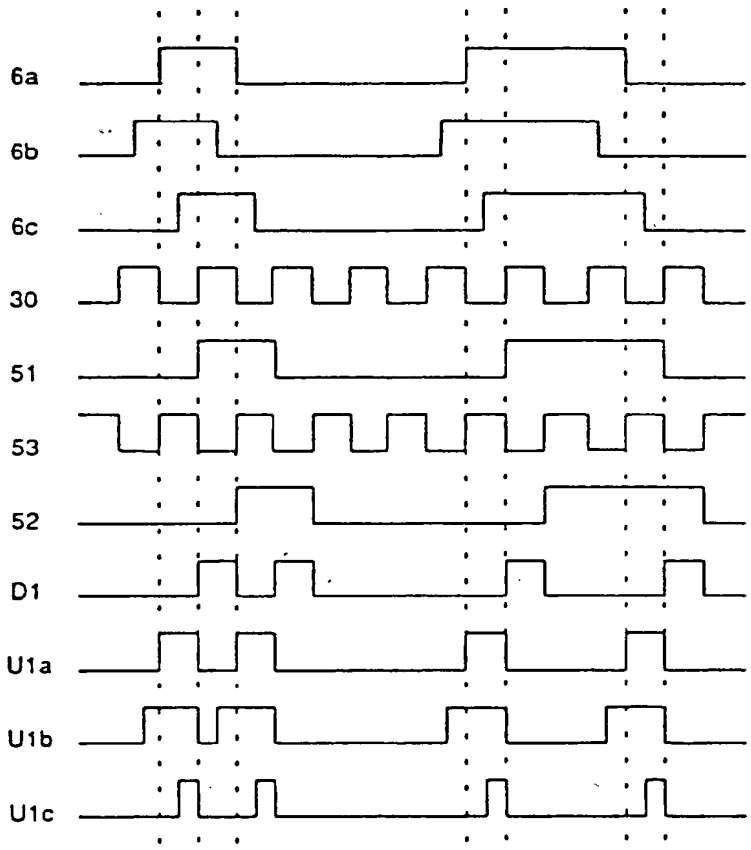
6a
6b
6c
30
51
53
52
D1
U1a
U1b
U1c

Fig. 6

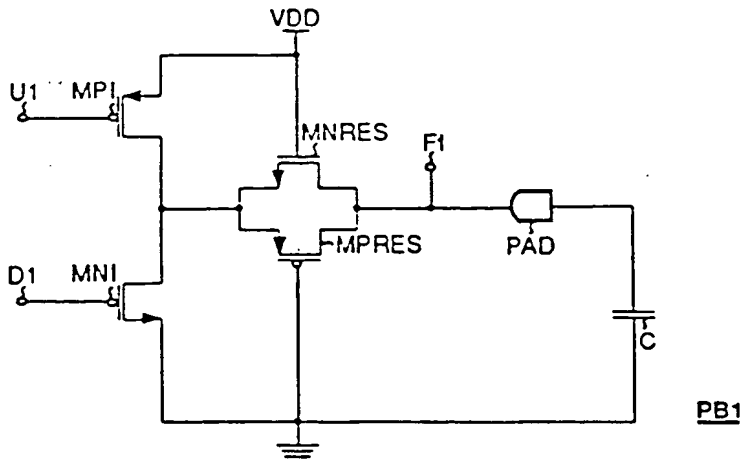
VDD
U1
MPI
MNRES
F1
MPRES
PAD
D1
MNI
C
PB1

Fig. 7

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EUROPEAN SEARCH REPORT

Application Number
EP 94 11 9838

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y A	US-A-5 015 970 (WILLIAMS ET AL) * column 2, line 28 - line 36 * * column 3, line 57 - column 4, line 4 * * column 4, line 14 - line 41 * * claims 1,5,9 * ---	1 2,3	H04L27/22 H04L7/033
Y	PATENT ABSTRACTS OF JAPAN vol. 18, no. 10 (E-1487) 10 January 1994 & JP-A-52 052 046 (NEC CORP) 28 September 1993 * abstract * ---	1	
D,A	PROCEEDINGS OF THE IEEE 1992 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 6 May 1992, BOSTON, MASSACHUSETTS pages 29.6.1 - 29.6.5 B.L. THOMPSON ET AL. 'A BICMOS RECEIVE/TRANSMIT PLL PAIR FOR SERIAL DATA COMMUNICATION' * page 29.6.1, right column, line 1 - page 29.6.2, left column, line 23 * * page 29.6.2, left column, line 23 - right column, line 10 * -----	1-3	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H04L
H03L
H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 March 1995	Canali, F

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